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SYNTHETIC TESTING OF LOAD CURRENT INTERRUPTION IN MEDIUM VOLTAGE LOAD BREAK SWITCHES

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Abstract. To conduct the mainly active load current test duty according to IEC 62271-103, a directly powered test circuit and therefore a medium voltage connection or a power generator is needed. A newly developed synthetic test circuit allows to replicate the current as well as the full transient recovery voltage (TRV) and the power frequent recovery voltage (RV) of the direct test circuit up to its crest value. It is dimensioned for voltage classes up to 52 kV and can be adapted to test currents between 630 A and 1250 A. The test circuit allows a detailed investigation of load break switches without costly high power sources and loads. Many parameters, like current and voltage steepness at current zero, as well as different parameters defining the TRV steepness can be varied individually.

Keywords: Load switching, synthetic testing, circuit simulation, load break switch.

1. Introduction

In todays medium voltage grids load break switches (LBS) are often used. In the voltage range from 1 kV to 52 kV they serve as an economical alternative to relatively expensive circuit breaker/disconnector combinations.

To improve present LBS as well as to develop future switchgear, an intensive experimental testing is necessary. For high voltage circuit breakers a synthetic test circuit is known, giving a high flexibility in current and voltage waveforms [1]. The type testing of LBS is standardized by IEC 62271-103 as the mainly active load current test duty TD_{load} with a directly powered test circuit [2]. To perform these tests a medium voltage connection or a high power generator is needed.

Previous investigations show different approaches in designing an easier, more flexible test by either modifying the direct test to only meet the IEC standard in the first few hundred microseconds after current zero (CZ) [3] or breaking the test down to a two-part synthetic test with one test for the first few hundred microseconds, the so-called transient recovery voltage (TRV), and one test for the latter part of the recovery voltage, the power frequent recovery voltage (RV) [4].

In this paper a newly developed synthetic test circuit for medium voltage LBS testing is presented. In a first step, the current and voltage forms in the IEC direct test are analyzed and the requirements for the synthetic test circuit are formulated. Afterwards, the design of the new test circuit is described in detail. The dimensioning is shown and results of circuit simulations carried out with MATLAB Simulink are compared to the test circuit requirements.

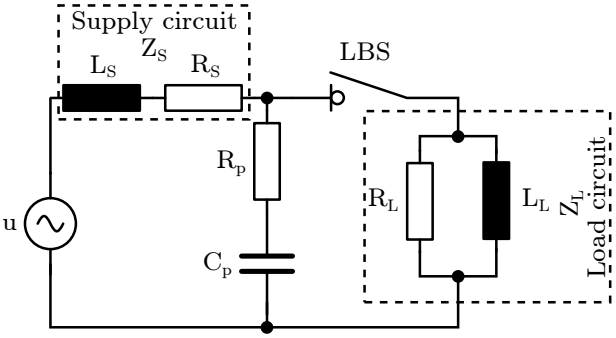

Figure 1. Circuit diagram of the single phase direct test circuit according to IEC 62271-103

2. Test circuit requirements

The direct test circuit specified in IEC 62271-103 is shown in Figure 1. It can be divided into a supply and a load circuit with the impedances Z_S and Z_L respectively. The voltage u is defined as $U_{Test} = k_{pp} \times U_r/\sqrt{3}$ with a first-pole-to-clear factor of $k_{pp} = 1.5$. The switching current is determined by the total impedance $Z_S + Z_L$ of the circuit. The ratio of the impedances is defined as $|Z_S| = (0.15 \pm 0.03)|Z_L|$. The power factor of the two impedances should be in the range of $\cos\varphi_S \leq 0.2$ and $0.65 \leq \cos\varphi_L \leq 0.75$, respectively. The parallel capacity as well as the resistor are chosen with regard to the rise time and peak value of the prospective TRV in case of a short-circuited load. The corresponding values are given in [2].

The direct test circuit is dimensioned for the voltages $U_r = 7.2$ kV, 12 kV, 24 kV, 36 kV and 52 kV. Simulations are carried out in MATLAB Simulink to ana-

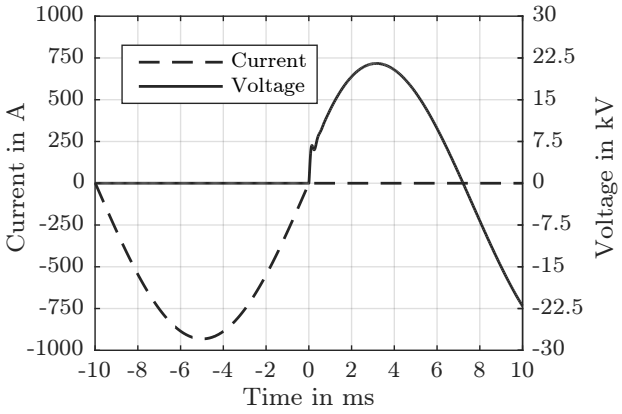

Figure 2. Current an voltage of simulated 24 kV direct test

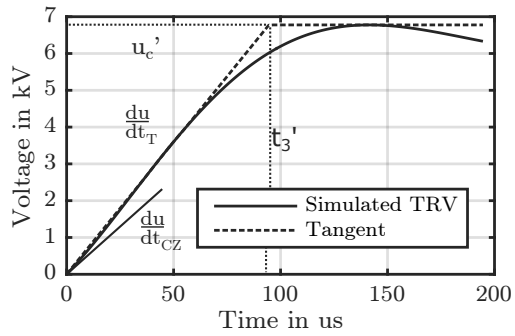

Figure 3. First 200 µs of the simulated TRV of the direct test circuit

lyze the shape of the resulting recovery voltage. The shape of the current as well as the recovery voltage for a test with a rated voltage of $U_\mathrm{r} = 24\,\mathrm{kV}$ and $I = 630\,\mathrm{A}$ are shown in Figure 2. The supply circuit has a power factor of $\cos\varphi = R_\mathrm{S}/Z_\mathrm{S} = 0.2$ and the load circuit has a power factor of $\cos\varphi = Z_\mathrm{L}/R_\mathrm{L} = 0.75$. The resulting recovery voltage is the difference of the voltage on the supply side, which is a fast rise to the grid voltage, and the voltage on the load side, an exponentially decaying DC-voltage. This leads to a two-step recovery voltage with a relatively steep first part until a first maximum plateau, the TRV, and a slower rising second part until the crest value, the RV.

The first 200 µs after CZ are shown in Figure 3. The shape of the TRV is analyzed as in [3] considering the maximum of the first peak u'_c, the voltage steepness at CZ $\mathrm{d}u/\mathrm{d}t_\mathrm{CZ}$ as well as the steepness of an aligned tangent $\mathrm{d}u/\mathrm{d}t_\mathrm{T}$ and the rise time t'_3. The tangent and rise time are defined as is [2]. The resulting values are shown in Table 1. Due to the slight $(1-\cos)$-form of the TRV, the voltage steepness at CZ is lower than the steepness of the tangent for all rated voltages.

The RV part is analyzed regarding the crest value of the voltage u_cr and the time at which the crest value occurs t_cr. The resulting values are shown in Table 2. The time is constant for all voltages as it is defined by the sine-wave of the grid voltage and not longer by the elements in the circuit. The crest values

U_r[kV]	u'_c[kV]	t'_3[µs]	$\frac{\mathrm{d}u}{\mathrm{d}t}_\mathrm{CZ}[\frac{\mathrm{V}}{\mu\mathrm{s}}]$	$\frac{\mathrm{d}u}{\mathrm{d}t}_\mathrm{T}[\frac{\mathrm{V}}{\mu\mathrm{s}}]$
7.2	1.85	54.3	29.2	34.3
12	3.13	63.8	43	49.5
24	6.8	94.6	62.24	71.6
36	10.65	118	77.9	90.92
52	16.6	155	93.2	107.1

Table 1. Characteristics of the first part of the TRV in a direct test

U_r[kV]	u_cr[kV]	t_cr[ms]
7.2	6.45	3.15
12	10.75	3.15
24	21.51	3.15
36	32.26	3.15
52	46.61	3.15

Table 2. Characteristics of the second part of the TRV in a direct test

are only 73 % in amplitude and occur later than the unaffected voltage peak $\hat{U} = \sqrt{2}U_\mathrm{r}/\sqrt{3} \times k_\mathrm{pp}$. Both effects can be explained by the decaying DC voltage in the load circuit. Measurement results could show a higher and earlier amplitude in comparison to the simulations, due to a lower DC voltage on the load site.

Besides these definitions for direct testing, other requirements for the synthetic test are derived from [1] as the following:

1. The arcing power should be the same as in the direct test
2. There should be no time interval between current and voltage stress
3. The TRV of the synthetic circuit should be the same as the standardized TRV but not less in the first 1/8 of a 50 Hz period
4. There should be no damping of the TRV by the post-arc current
5. A switch failure should be clearly detectable.

3. Design of a synthetic test circuit

The novel synthetic test circuit for load break switches is a combination of three individual circuits. One circuit provides the high current and two circuits are shaping the recovery voltage. To avoid a gap between current and voltage stress, the current-superposition-method is chosen. Shortly before CZ a smaller current with a higher frequency is superimposed over the high current. While the high current is then interrupted by an auxiliary breaker, the superimposed current – with a slightly later CZ – is interrupted by the device under test. The final circuit diagram of the synthetic test circuit is shown in Figure 4. For reasons of simplicity, only a single phase test circuit is designed.

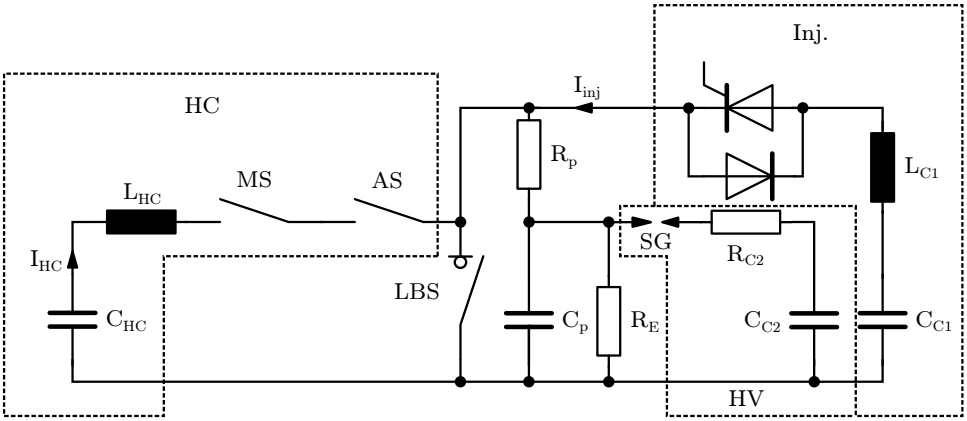

Figure 4. Circuit diagram of the synthetic test circuit

The high current (HC) circuit is a simple LC resonant circuit containing a making switch (MS) and an auxiliary switch (AS). The frequency of this circuit is determined by the values of C_{HC} and L_{HC} and should be set to nearly 50 Hz. Additionally the elements should be chosen in a way, that the charging voltage for a certain test current is significantly above the arcing voltage of the test device to avoid damping of the current.

As the current I_{HC} approaches CZ the thyristor in the injection circuit (Inj.) is fired, injecting the superimposed current I_{inj} into the test object. The value of the inductance L_{C1} is determined by the steepness of the injection current at current zero:

$$\frac{\mathrm{d}i_{\mathrm{Inj}}}{\mathrm{d}t}|_{t=t_{\mathrm{CZ}}} \stackrel{!}{=} \frac{\mathrm{d}i_{\mathrm{HC}}}{\mathrm{d}t}|_{t=t_{\mathrm{CZ}}}, \tag{1}$$

$$\frac{\mathrm{d}i_{\mathrm{Inj}}}{\mathrm{d}t}|_{t=t_{\mathrm{CZ}}} = \frac{U_{C_{\mathrm{C1}}}|_{t=t_0}}{L_{\mathrm{C1}}} \tag{2}$$

After the current is successfully interrupted, the capacitance C_{C1} is charged negatively and the first part of the TRV is applied to the test object through C_{C1}, L_{C1} and the parallel elements R_{p} and C_{p}. The thyristor is now changing back to blocking mode and the charging current is carried by the free wheeling diode until the first maximum of the TRV is crossed. The voltage steepness at CZ is only defined by the value of R_{p}:

$$\frac{\mathrm{d}u}{\mathrm{d}t}|_{t=t_{\mathrm{CZ}}} = R_{\mathrm{p}} \times \frac{\mathrm{d}i_{\mathrm{Inj}}}{\mathrm{d}t}|_{t=t_{\mathrm{CZ}}} \tag{3}$$

The voltage shape until the first maximum is dependent on all the components and, as C_{C1}, L_{C1} and R_{p} are set, can be influenced by changing the value of C_{p}.

As soon as the TRV crossed its first peak, the diode is blocking and the spark gap (SG) of the high voltage circuit (HV) is triggered. The capacitance C_{C2} is negatively charged and therefore the absolute value of the recovery voltage rises to its crest value. The rise time is defined by the resistor R_{C2}. The resistor R_{E} is a discharge resistor and does not affect the highly transient events in the first few milliseconds after CZ.

U_r [kV]	L_{C1} [mH]	R_{p} [Ω]	U_{C1} [kV]	U_{C2} [kV]
7.2	5.18	107	1.45	7
12	8.93	155	2.5	11.5
24	19.29	225	5.4	23
36	30.36	278	8.5	34.4
52	46.43	332	13	50

Table 3. Component values and charging voltages for the synthetic test circuit

3.1. Dimensioning

The dimensioning of the circuit is obtained partly analytical using the above equations and partly using the simulation software MATLAB Simulink. For the high current circuit a charging voltage of $U_{\mathrm{c}} = 1\,\mathrm{kV}$ for a test current of $I = 630\,\mathrm{A}$ is chosen to be significantly above the arcing voltage of the test object. This leads to an inductance of $L_{\mathrm{HC}} = 3.57\,\mathrm{mH}$ and a capacitance of $C_{\mathrm{HC}} = 2.8\,\mathrm{mF}$. The values of the three capacitances C_{p}, C_{C1} and C_{C2} are constant for all rated voltages with $C_{\mathrm{p}} = 160\,\mathrm{nF}$, $C_{\mathrm{C2}} = 3.88\,\mu\mathrm{F}$ and $C_{\mathrm{C1}} = 1\,\mu\mathrm{F}$ respectively.

As the rise time for the RV is constant as well (s. Table 2), the resistor R_{C2} is consequently determined for all voltage levels with $R_{\mathrm{C2}} = 6.3\,\mathrm{k\Omega}$. Due to the different voltage steepnesses for the different levels the values of L_{C1} and R_{p} as well as the charging voltages for the capacitances C_{C1} and C_{C2} have to be chosen individually. The calculated values are shown in Table 3.

3.2. Simulative analysis

The voltage waveform of the resulting TRV of the synthetic test circuit is analyzed regarding the same characteristics as in section 2. The resulting values for the different voltage levels are shown in Table 4. As in Table 1 the tangent steepness is higher than the voltage steepness at CZ due to the $(1-\cos)$-form. The values show a high correspondence to the results of the direct test, with a smaller rise time t_3 and therefore a higher tangent steepness $\mathrm{d}u/\mathrm{d}t_{\mathrm{T}}$ for all rated voltages.

U_r[kV]	u'_c[kV]	t'_3[µs]	$\frac{\mathrm{d}u}{\mathrm{d}t}_{\mathrm{CZ}}[\frac{\mathrm{V}}{\mu\mathrm{s}}]$	$\frac{\mathrm{d}u}{\mathrm{d}t}_{\mathrm{T}}[\frac{\mathrm{V}}{\mu\mathrm{s}}]$
7.2	1.87	50.97	30.02	37.13
12	3.18	63.32	43.46	50.43
24	6.88	93.25	63.02	74.14
36	10.86	117.8	77.96	92.59
52	16.71	148.1	93	113.3

Table 4. Characteristics of the first part of the TRV in a synthetic test

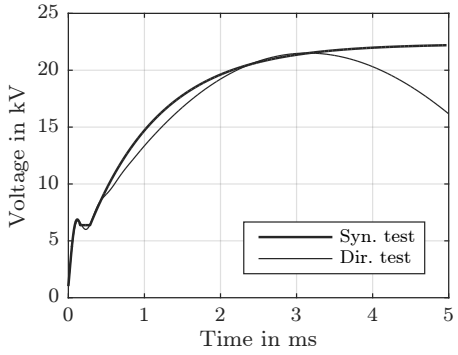

Figure 5. Comparison of the TRV of the synthetic test circuit and the direct test

Maximum u'_c and voltage steepness at CZ $\mathrm{d}u/\mathrm{d}t_{\mathrm{CZ}}$ are nearly identical to the direct test.

The RV meets the exact requirements shown in Table 2 for all voltage levels but shows a higher steepness in the beginning due to its exponential character.

4. Discussion

Figure 5 shows the comparison of the recovery voltage of the synthetic test circuit and the standardized direct test circuit. The first 150 µs are shown in Figure 6. For the first 50 µs the voltages of the two circuits show no significant difference. Afterwards the TRV of the synthetic test is slightly above the the TRV of the direct test, which leads to the higher tangent steepness and the lower rise time. In the RV part the voltage of the synthetic circuit is rising faster due to its exponential character. Both leads to test conditions which are equal or harder than in the direct test and therefore fulfills the requirements defined in section 2. After the crest value, the voltage of the synthetic test circuit is nearly constant while the voltage of the direct test circuit decreases and approximates the grid sine-wave. However, during this time-period, the critical dielectric phase for the LBS is assumed to have ended.

A limitation of the synthetic test is, as for synthetic testing of circuit breakers, that the load break switch must interrupt the current in the first half wave, due to the polarity of U_{C2}. It is possible to redesign the test in a way, that current interruption in the second half wave is tested. But in that case the switch must not clear in the first half wave. This can be archived

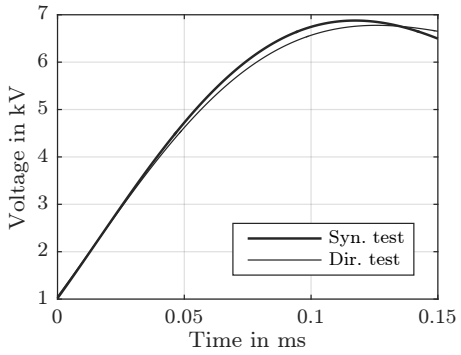

Figure 6. First 150 µs of the TRVs of the synthetic and the direct test

by an additional re-ignition circuit. Furthermore, a natural damping occurs in the test circuit. Therefore, if multiple current zero crossings are tested, the current's amplitude as well as its steepness at current zero decrease with every current zero crossing.

5. Conclusion

The proposed synthetic test circuit for load current interruption tests of medium voltage load break switches offers a highly flexible and cheap alternative to the standardized direct test. Simulations in MATLAB Simulink show a high correspondence of the different TRV characteristics with the direct test. The shape of the recovery voltage can be easily changed and adapted, as i.e. the two parts – TRV and RV – can be varied individually. The synthetic test circuit has the limitation that the current interruption must take place in a predefined half wave.

Acknowledgements

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References

[1] IEC 62271-101:2012 High-voltage switchgear and controlgear - Part 101: Synthetic testing. Standard, International Electrotechnical Comission, 06 2012.

[2] IEC 62271-103:2011 High-voltage switchgear and controlgear - Part 103: Switches for rated voltages above 1 kV up to and including 52 kV. Standard, International Electrotechnical Comission, 06 2011.

[3] E. Jonsson and M. Runde. Medium voltage laboratory for load break switch development. In *International Conference on Power System Transients*, 07 2013.

[4] A. Islam, D. Birtwhistle, T. K. Saha, and B. Diverall. Two-part synthetic test procedures for the testing of medium-voltage load break switches. In *IEEE Transactions on Power Delivery*, volume 31, pages 1645–1654, 08 2016. doi:10.1109/TPWRD.2015.2511188.